REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 9-14 and 16-24 are currently pending. Claims 16 and 22 have been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claim 22 was objected to as being indefinite regarding the term "external input signal"; Claims 16, 21, and 22 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement regarding the first and second reference signals being inputted from outside the semiconductor apparatus; Claim 22 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0199841 to Marr (hereinafter "the '841 application"); Claims 16-18 and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Applicants' admitted prior art" (hereinafter "the Background Art"); in view of the '841 application; Claims 19 and 20 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form; and Claims 9-14, 23, and 24 were allowed.

Applicants respectfully submit that the objection to Claim 22 is rendered moot in part by the present amendment to Claim 22 and is otherwise traversed. Claim 22 has been amended to refer only to an external input signal rather than also to an input signal. Further, Applicants note that Figure 7 shows an external input signal Vin, as admitted in the Office Action. Accordingly, the objection to Claim 22 is believed to have been overcome.

Applicants respectfully traverse the rejection of Claims 16, 21, and 22 under 35 U.S.C. § 112, first paragraph. As shown in Figure 5, the first and second reference signals Vref0 and Vref1 are inputted from outside of the semiconductor apparatus. As shown in

Figure 5, the first and second reference signals Vref0 and Vref1 are transmitted via first and second voltage supplying lines 13 and 14 connected to the semiconductor apparatuses 10. Accordingly, Applicants submit that it is clear that the first and second reference signals are inputted from outside the semiconductor apparatus. See also pages 10 and 11 of the specification.

Claim 22 is directed to a semiconductor apparatus having a logic level decision circuit, the logic level decision circuit comprising: (1) a first comparison circuit which compares an external input signal with a first reference signal corresponding to a logic "1" level, and which outputs a first differential signal; (2) a second comparison circuit which compares the external input signal with a second reference signal corresponding to a logic "0" level, and which outputs a second differential signal; and (3) a third comparison circuit which compares the output of the first comparison circuit and the output of the second comparison circuit, and which outputs one of the logic "1" level and the logic "0" level. Further, Claim 22 recites that the output of the third comparison circuit follows the external input signal, and the first and second reference signals are inputted from outside of the semiconductor apparatus. The changes to Claim 22 are supported by the originally filed specification and do not add new matter.

The '841 application is directed to a midpoint detection circuit 200 that generates a midpoint signal MS by detecting the midpoint of an input signal SIN in order to enter a test mode. As shown in Figure 3, the '841 application shows another embodiment of the midpoint detection circuit shown in Figure 2A of the '841 application. As shown in Figure 3, the '841 application discloses that the midpoint detection circuit 200 has reference voltages Vref1 and Vref2 supplied to a pair of differential amplifiers 222 and 224, respectively. Thus, the '841 application discloses that the circuit shown in Figures 2A and 3 changes a logic level of the output signal according to whether a voltage level of an input signal is at midpoint or

not. Thus, if the voltage level of the input signal is not at the midpoint MP, but close to a value VCC or close to ground, the logic level of the output signal has the same level. However, Applicants respectfully submit that the '841 application fails to disclose a third comparison circuit which compares the output of the first comparison circuit and the output of the second comparison circuit, and which outputs one of the logic "1" level and the logic "0" level, wherein the output of the third comparison circuit follows the external input signal and the first and second reference signals are input from outside the semiconductor apparatus, as recited in Claim 22. Accordingly, Applicants respectfully submit that the rejection of Claim 22 is rendered moot by the present amendment to that claim.

Amended Claim 16 is directed to a signal transmission system which transmits and receives binary logic signals between a plurality of semiconductor apparatuses, wherein the plurality of semiconductor apparatuses respectively have an input receiver that decides a logic level of an external input signal, and a first reference signal corresponding to a logic "1" level of the input signal and a second reference signal corresponding to a logic "0" level are supplied as reference signals for logic level decision to the respective input receivers. Further, Claim 16 has been amended to clarify that the respective input receivers output one of the logic "1" level and the logic "0" level, and the output of the respective input receivers follows the external input signal. Further, Claim 16 recites that the first and second reference signals are inputted from outside of the plurality of semiconductor apparatuses. The changes to Claim 16 are supported by the originally filed specification and do not add new matter.

Regarding the rejection of Claim 16 under 35 U.S.C. § 103, the Office Action asserts that the Background Art discloses everything in Claim 16 with the exception of the first and second reference voltages, and relies on the '841 application to remedy those deficiencies.

Figure 1 of the Background Art is directed to a conventional inter-semiconductor apparatus signal transmission system in which a plurality of semiconductor apparatuses 100

have address/data bus and control signal lines 11 attached to them. Further, the Background Art discloses that a reference voltage Vref transmitted on a voltage supplying line 12 has an intermediate value of the voltage of the logic level "1" level and the voltage of the logic level "0" level of a binary input signal. However, as admitted in the Office Action, the Background Art fails to disclose first and second reference voltage signals supplied as reference signals for logic level decision to respective input receivers, as recited in Claim 16. Further, Applicants respectfully submit that the Background Art fails to disclose that the respective input receivers output one of the logic level "1" and the logic level "0" level and the output of the respective input receivers follows the external input signal, as recited in Claim 16.

As discussed above, the '841 application is directed to a midpoint detection circuit 200 that generates a midpoint signal MS by detecting the midpoint of an input signal SIN in order to enter a test mode. The '841 application discloses that Vref1 and Vref2 signals are generated inside the chip. The '841 application discloses an intermediate level between the logic level "1" and the logic level "0" in order to enter a test mode. However, Applicants respectfully submit that the '841 application fails to disclose the first and second reference signals are inputted from outside of the plurality of semiconductor apparatuses and that the respective input receivers output one of the logic level "1" level and the logic "0" level, and the output of the respective input receivers follows the external input signal, as recited in Claim 16. Rather, as discussed above, the '841 application is directed to detecting the midpoint of an input signal.

Thus, no matter how the teachings of the Background Art and the '841 application are combined, the combination does not teach or suggest first and second reference signals that are inputted from outside of a plurality of semiconductor apparatuses, and respective input receivers of the plurality of semiconductor apparatuses output one of the logic "1" level and

the logic "0" level, and the output of the respective input receivers follows the external input signal, as recited in Claim 16. Accordingly, Applicants respectfully submit that the rejections of Claim 16 (and dependent Claims 17 and 18) are rendered moot by the present amendment to Claim 16.

Claim 21 recites limitations analogous to the limitations recited in Claim 16. Accordingly, for the reasons stated above for the patentability of Claim 16, Applicants respectfully traverse the rejection of Claim 21 under 35 U.S.C. § 103.

Thus, it is respectfully submitted that independent Claims 16, 21, and 22 (and all associated dependent claims) patentably define over any proper combination of the '841 application and the Background Art.

Consequently, in view of the present amendment and in light of the following discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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